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Low Power 1-Bit Full Adder Using Full-Swing Gate Diffusion Input Technique

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Abstract

This paper presents a design which provides full swing output for logic 1 and logic 0 for 1-bit full adder cell and reduces power consumption, delay, and area. In this design full adder consists of two XOR gate cells and one cell of 2x1 multiplexer (MUX). The performance of the proposed design compared with the different logic style for full adders through cadence virtuoso simulation based on TSMC 65nm technology models with a supply voltage of 1v and frequency 125MHz. The simulation results showed that the proposed full adder design dissipates low power, while improving delay and area among all the design taken for comparison.

Keywords— Full adder; Gate Diffusion Input (GDI); FS-GDI.

I. INTRODUCTION

Lately, the rapid advance in multimedia and digital communication systems, real time signal processing like audio signal processing, image and video processing are heavily needed. Many applications such as Processors and Digital Signal Processing operations such as Filtering, Convolutional transformation, require some form of addition such as multiplication, multiply and accumulate operation (MAC) and subtraction. The 1-bit full adder cell is the main block in all these modules [1]. Because of the need in portable devices such as laptop and cell phones for low power consumption. The power consumption, small area and high speed are the crucial factors to be considered in VLSI design with high performance [2]. There were many techniques to design in VLSI circuit and minimize the power and area, but their best gate diffusion input technique The aim of this work is to design 1-bit full adder circuit using full-swing GDI to reduce power consumption, delay and area, in addition to achieve full-swing output This paper is organized as follows: Section II overviews the GDI methodology and

presents its benefits and limitations. The design of The Full Adder Cell is discussed in Section III. Section IV presents simulation results and comparison. Section V concludes the paper. II. GATE DIFUSSION INPUT TECHNIQUE In 2002 [3] A. Morgenshtein, A. Fish and A. Wagner proposed Gate Diffusion Input Technique (GDI) for low power and small silicon area of VLSI digital design as an alternative to CMOS logic design. Presented in figure 1 (a) Primitive Proposed GDI cell

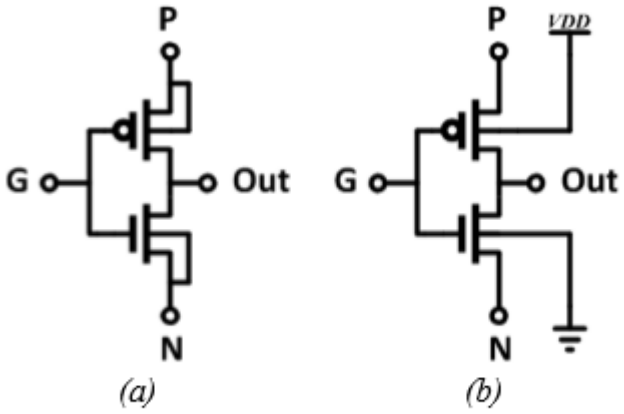

Fig.1. GDI cell; (a) Primitive Proposed GDI Cell, (b) MOD-GDI

Actually, this technique proposed for fabrication in silicon on insulator (SOI) and twin-well CMOS processes. Also, it provides an effective way for the design of fast, low power design using less number of transistors as compared to CMOS, PTL and TG techniques. This allows the design of many complex functions using only 2 transistors as listed in table I.

TABLE I. Different logic functions realization using GDI cell

N	P	G	OUT	Function
0	B	A	$\bar{A}B$	F1
B	1	A	$\bar{}$+B	F2
1	B	A	A+B	OR
B	0	A	AB	AND
C	B	A	$\bar{A}B$+AC	MUX
0	1	A	$\bar{}$	NOT

This logic style was suffering from some limitations such as reduced output voltage swing due to the threshold drops, this means that the output either high or low voltage is deviated from

VDD or GND by threshold voltage drop (Vth), as that threshold drop causes performance degradation and increases short circuit power. To solve this problem Morgenshtein, Shwartz and Fish [4] proposed modified gate diffusion input logic style (MODGDI) the cell is similar to basic cell of GDI, but have important difference in MOD-GDI, the substrate terminals of NMOS and PMOS connected to GND and VDD, respectively, as shown in figure 1(b). This logic is compatible for implementation in a standard CMOS process, and achieves improvement in output, power and power delay product compared to the basic GDI logic. W, while the threshold drop problem, not fully resolved, but the output still has degraded still degrades the output. In [5] Morgenshtin proposed a new approach to improve the output swing and overcome the threshold drop problem known as Full Swing (FS) GDI technique and utilizes only swing restoration transistor (SR) to ensure the full swing operation for F1 and F2 function. Either F1 or F2 gates or a combination of both can be used to realize any logical function. Although this technique uses more transistors than standard GDI but compared to CMOS logic style it uses a fewer number of transistors and achieves full swing output, low power, less delay and small area of the circuit. III. FULL ADDER In this paper the Full-Swing GDI technique is used to realize the circuits required to design the Full Adder as follows: A. XOR Gate XOR gate is the basic building block for the realization of various digital circuits such as multiplier, comparator, adder, decoder, and compressor[6]. The design XOR gate requires 4 transistors as shown in fig 2(a). The output can be expressed as:

$$A \text{ XOR } B = A \oplus B = \bar{A}B + A\bar{B} \qquad (1)$$

At A=0, B=0 the NMOS transistor is switched off and PMOS transistor is switched on, where PMOS in the linear region. At Vin–Vtp < Vout < VDD, NMOS is cut off Vin< Vtn, then the output of XOR gate equal to (Vtp) threshold voltage of PMOS transistor. At A=0, B=1 NMOS is cut off Vin< Vth, the PMOS in the linear region Vin–Vth < Vout < VDD, then the output of XOR equal to VDD passes through PMOS. At A=1, B=0 the PMOS transistor is switched off and NMOS transistor is switched on, where PMOS is cut off Vin<Vtp and NMOS in the linear region Vin–Vtn < Vout < VDD then the output of the XOR gate is equal to VDD-Vtn, (Vtn) threshold voltage of NMOS transistor. At A=1, B=1 PMOS is cut off and NMOS in the linear

region, then the output equal to ground passes through NMOS. The operation of XOR gate summarized at table II We notice the disadvantages of the output in figure(7) to solve this problem using NMOS to delivering strong zero and PMOS to delivering strong one, shown in figure 2(b),wave form shown in figure (8).

TABLE II. Truth Table Of XOR Gate.

A	B	A XOR B
0	0	Vtp
0	1	VDD
1	0	VDD-Vtn
1	1	GND

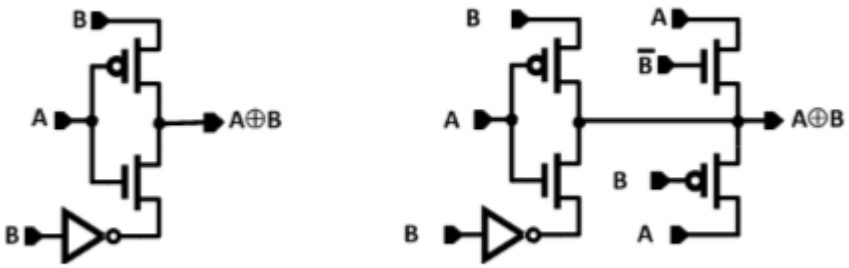

Fig.2. GDI cell; (a) 4T-XOR GATE, (b) 6T-XOR GATE

B. 2×1 Multiplexer The basic MUX has a number of information input-lines and one output line. A multiplexer chooses the output from multi information inputs based on a select signal, shown in Fig. 3 a 2×1 Multiplexer consists of 6 transistors[7].

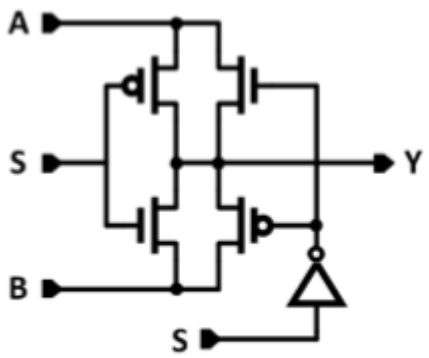

Fig.3. Full-Swing GDI 2x1 Multiplexer

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C. Design of Full Adder A full adder is a combinational circuit that performs the arithmetic operation of 3 number of bits [8]. Addition considered an essential operation in arithmetic and logic unit digital signal processing and. The 1-bit full adder contains three input bits and two output bits, the first two bits of the inputs are A and B called operands and the third input bit Cin is a bit carried in from the previous less-significant stage, output bits called sum is the result of addition operation and carry out which will be the input carry to the next addition operation, and the expression:

$$SUM = A \oplus B \oplus Cin \qquad (2)$$

$$COUT = A\,\overline{(A \oplus B)} + Cin\,(A \oplus B) \qquad (3)$$

The proposed design consists of 16 transistors including two XOR gate cells to produce sum and one multiplexer cell to produce carry out, as shown in figure (4), the block diagram shown in figure (5), and the truth table of proposed full adder presented in table III

Table III. Truth Table Of Proposed Full Adder

A	B	Cin	SUM	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

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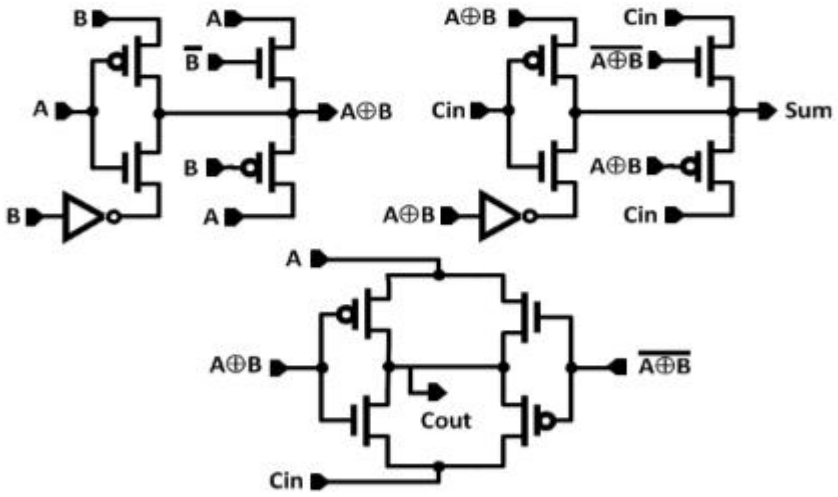

Fig.4. Proposed design for 1-Bit Full Adder

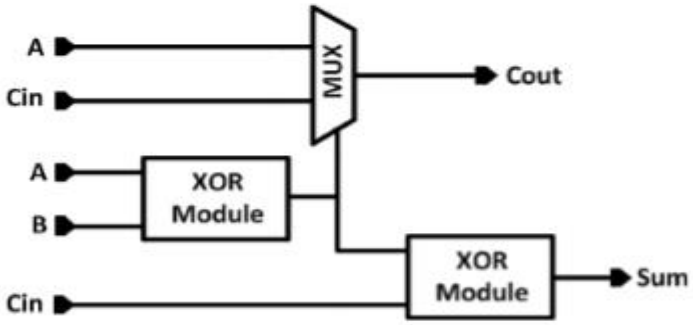

Fig. 5. Block Diagram For Proposed Full Adder

IV. SIMULATION RESULTS AND COMPARISON

The proposed 1-bit Full Adder circuit was designed in 65nm TSMC process. The simulations were done using the SPECTRE based Cadence Virtuoso simulator with a power

supply of 1V and frequency 125MHz, the size of PMOS is twice the NMOS transistor size Wp/L=240/60, Wn/L=120/60 (PMOS and NMOS respectivily) to achieve the best power and delay performance. Fig.8 shows the waveform of the proposed Full Adder, The results of the proposed design compared with the designs in References [4] , [5] and [6] are shown in Table III. Compared to the previous designs, the proposed design for 1-bit full adder consumes low power as that needed to least number of transistors to building circuits and present full swing output and less delay.

TABLE IV. Simulation Results.

Design	No.of Transistors	Power (nW)	Delay (ps)	Supply Voltage	Technology
Shoba.2016[9] Design1	18	927.9 nW	37.86	1.1V	45nm
D.shindi [10]	10	8100 nW	6.47	-	45nm
Shoba 2014 [11]	21	9000 nW	18	1.2	120nm
Proposed Design	16	693.5 nW	2.5	1V	65nm

V. CONCLUSION

This work presents a 1-bit Full Adder designed in 65nm TSMC process using the Full-Swing GDI technique and simulated using the Cadence Virtuoso simulator. Simulation results showed design in terms of power consumption and transistor count, while maintaining Full-Swing Operation. The proposed design consists of 16 transistors and operates under 1V supply voltage.

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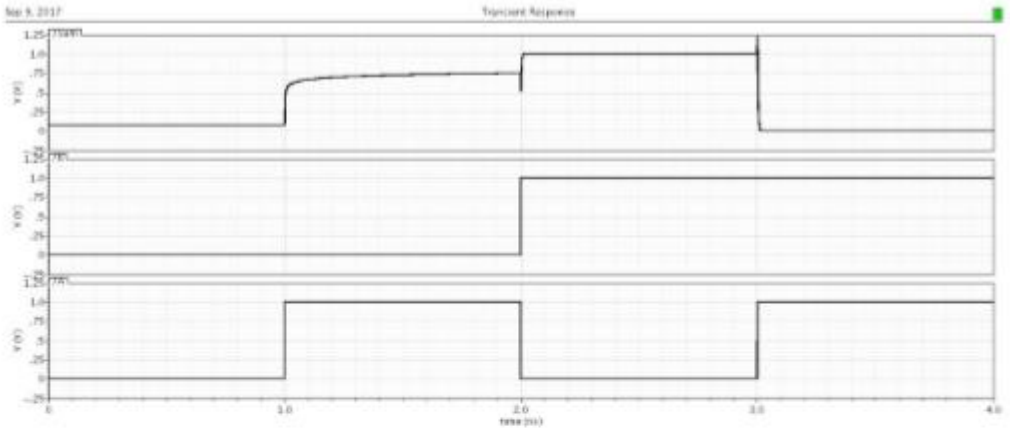

Fig.6. Waveform of 4T-XOR Gate

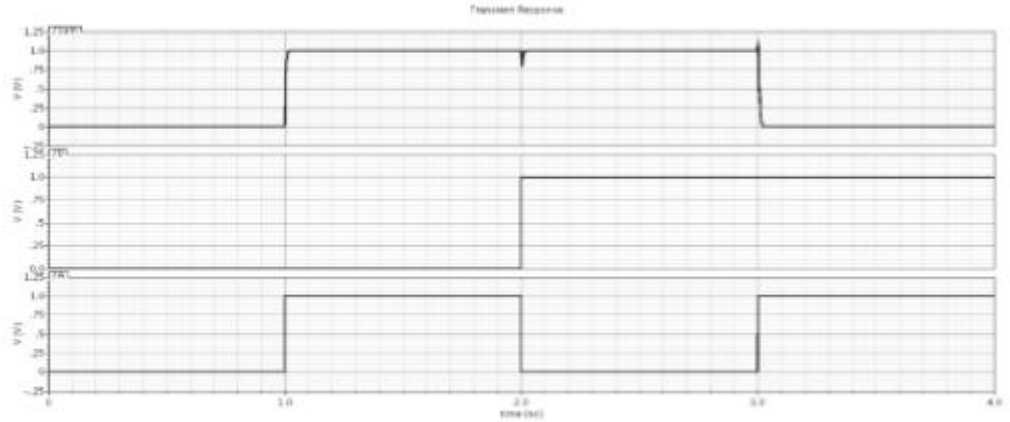

Fig.7. Waveform of 6T-XOR Gate

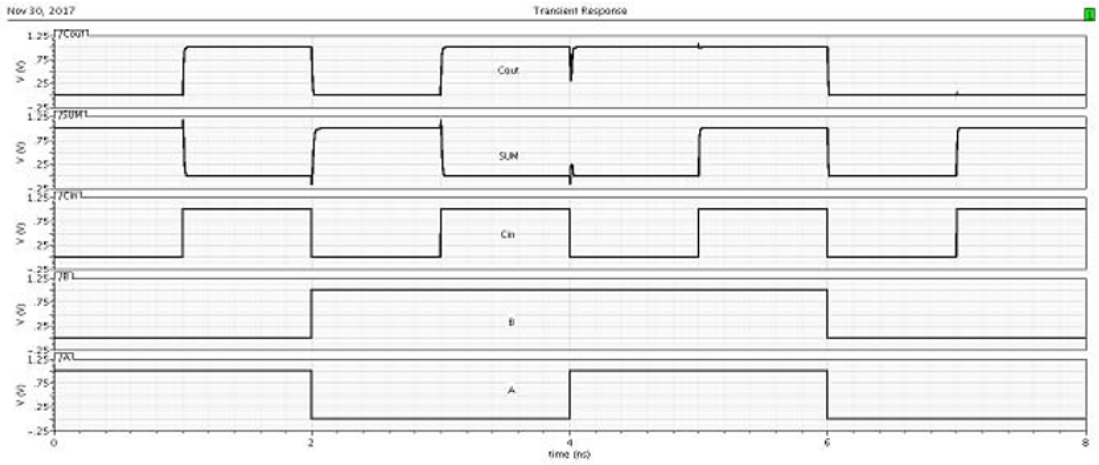

Fig.8.Output Waveform of the Proposed Design

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