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Photovoltaic Source Simulator Fast Time Response for Solar Power Conditioning Systems Evaluation

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***Abstract*—**Photovoltaic (PV) source simulators serve as a conve-nient tool for the dynamic evaluation of solar power conditioning systems and maximum power point tracking algorithms. High ef-ficiency and fast transient response time are essential features of any PV source simulator. This paper proposes a new type of PV source simulator that incorporates the advantages of both ana-log and digital-based simulators. The proposed system includes a three-phase ac–dc dual boost rectifier cascaded with a three-phase dc–dc interleaved buck converter. The selected power stage topology is highly reliable and efficient. Moreover, the multiphase converter helps improve system transient response though pro-ducing low output ripple which makes it adequate for PV source simulators. The simulator circuitry emulates precisely the static and the dynamic characteristics of actual PV generators under different load and environmental conditions. Additionally, the sys-tem allows the creation of the partial shading and bypass diodes effect on PV characteristics. The paper investigates the dynamic performance of a commercial solar power inverter using the pro-posed PV source simulator in steady-state and transient conditions. Closed-loop output impedance of the proposed PV source simula-tor has been measured and verified at different operating regions. The impedance profile—magnitude and phase—matches the out-put impedance of actual PV generators.

I INTRODUCTION

Solar or PV cells are used to directly convert sunlight into dc power. Solar cells exhibit nonlinear output current–voltage characteristics. This current–voltage curve is characterized with a unique maximum power point (MPP) and depends on envi-ronmental conditions (solar irradiance, cell temperature, wind speed, etc.) and PV cell fabrication material [5]–[7]. Accord-ingly, a maximum power point tracking (MPPT) algorithm is required in solar power conditioning systems in order to max-imize the generated output power [8]–[12]. Testing medium-and high-power solar power conditioning systems with actual solar cells along with direct solar irradiance or an artificial light source is costly, bulky, and highly dependent on weather con-ditions. Furthermore, evaluation and comparison of different MPPT techniques requires repeatable weather and load condi-tions that are impractical. To overcome these difficulties, PV source simulators have been introduced.

A PV source simulator is a power electronics circuit able to reproduce the static and the dynamic output characteristics of an actual solar cell or arrays of cells over a wide range of environmental and load conditions. PV source simulators can be cost-effective, compact, and flexible [13]. A well-designed PV source simulator should adopt the following features:

1) Accurately predict the static characteristics of solar cells and arrays under different environmental and load conditions.

2) Match the frequency response of the output impedance of actual PV cell in high- and low-frequency ranges and at different operating regions including constant current and constant voltage.

3) Simulate the PV characteristics under partial shading con-ditions with multiple peaks and steps.

4) Emulate the effect of bypass and blocking diodes on PV output characteristics.

5) Reflect the effect of different PV configurations on PV output characteristics.

6) Evaluate different MPPT algorithms performance with reasonable response time.

Achieve high power stage efficiency to be adequate for operations over a long period of equipment testing.

8) Interface capability with other power electronics circuits and solar power conditioning systems.

9) Evaluate solar power conditioning systems performance in steady-state and transient-state under different load and environmental conditions.

PV source simulators can be used to assess the PV energy pro-duction, experimentally investigate the dynamic performance of PV systems including stand-alone and grid-connected inverters regardless of environmental conditions, and evaluate different MPPT algorithms' response and efficiency.

PV source simulators can be classified into different cate-gories based on the design of power stage, control system, and reference generation technique. Power stage design can be con-figured with a linear [14], [15] or a switching power stage. Linear PV source simulators are excellent in dynamic response but are limited to low power applications. Low efficiency, high heat generation, and bulky size are serious concerns at high power applications where switching power stages are more attractive. To replicate the current–voltage characteristics of a PV cell, the switching power stage should operate in buck mode. Different switching power stages have been reported as PV source sim-ulators such as, single-phase dc–dc buck converter [16], three-phase ac–dc voltage source and current source rectifier [17], half- and-full bridge dc–dc converter [18], [19], and an LLC resonant dc–dc converter [20]. Other power stages have been used such as a dc programmable power supply with a current limit, dc power supply with a variable resistor [21] or controlled switch resistor [22], and active power load [23].

The reference current–voltage generation techniques can be either analog [24]–[26] or digital based [27]–[29]. The analog-based simulators are distinguished with simplicity and low cost implementation. Their current–voltage reference curves can be employed in one of three ways: 1) using a small PV cell with a light source [30]; 2) using a photodiode with a light-emitting diode [31]; and 3) using a PV cell diode model with current source [32], [33]. The first approach is a real-time simulator [34] and, hence, is the most accurate among other approaches. The second approach is flexible and can be used to emulate shading conditions effectively [35]. The implementation of the last ap-proach is simple where the current source represents the sunlight illumination. Digital reference generation based PV source sim-ulators are flexible, reliable, and less sensitive to high-frequency switching noise. However, the digital time delay may affect the performance and design of control loops. The current–voltage digital reference curve can be generated using one of two tech-niques. The first technique is to store premeasured current– voltage curves in a data memory at different environmental and load conditions [36]–[39]. The more data points stored, the higher the resolution and accuracy needs to be of the pregener-ated characteristics. The second technique is the digital imple-mentation of the mathematical model of PV cells [40]–[42]. A high-speed digital signal processor (DSP) is required due to the execution of sophisticated mathematical semiconductor equa-tions. Two PV models have been widely used: 1) the parametric model and 2) the interpolation model [43], [44]. The parametric model is used when all PV cell parameters (from manufacturer's data sheets) are known [45], whereas the interpolation model

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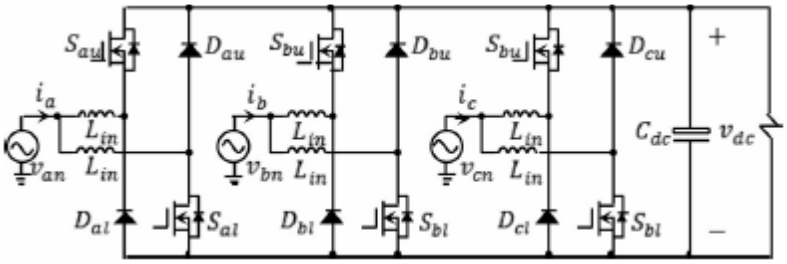

Circuit diagram of the proposed three-phase ac–dc dual boost rectifier.

requires knowledge of the open-circuit voltage, short-circuit current, voltage at the MPP, and current at the MPP [46], [47].

This paper presents a new type of PV source simulator. The proposed two-stage PV source simulator is characterized with high power stage efficiency and fast transient response time. Therefore, the proposed system is adequate for solar power conditioning systems evaluation. Response time of PV source simulators has been reported to be in the range of 10 ms to several 100 ms [48]–[50]. The hybrid simulator combines both analog- and digital-based concepts. This technique decreases digital computational times allowing a higher switching frequency, and therefore, a higher control loop bandwidth to be selected. The proposed system extracts real-time current–voltage refer-ence characteristics curves using an actual solar reference cell (0.5 W) with a controllable light source. This analog extraction technique is simple, very accurate, and flexible. Subsequently, the reference curves are processed with a DSP for flexible and reliable control loop implementation. The new switching power stage amplifies the reference curves with a pulsewidth modula-tor (PWM) to produce high-power current–voltage characteris-tics. The power stage consists of a three-phase active-front-end (AEF) ac–dc rectifier cascaded with a multiphase dc–dc in-terleaved converter. This paper describes the development and design of the PV source simulator in detail. System description along with control strategy will be thoroughly presented. Fur-thermore, the design methodology of the power stage and con-trol systems will be discussed.

II. SYSTEM DESCRIPTION AND CONTROL STRATEGY

The basic structure of the proposed PV source simulator is composed of three main circuit: 1) power stage circuit, 2) digital control circuit, and 3) analog reference-generation circuit. The power stage is a three-phase ac–dc rectifier cascaded with a multiphase dc–dc converter. The three-phase ac–dc rectifier is a new type of dual boost topology [51], [52]. Fig. 1 presents the circuit diagram of the proposed ac–dc dual boost rectifier. For each phase, the upper and lower switch duty cycles are determined by the direction of its input phase reference current

$$\left.\begin{aligned} i_{a_{ref}} &\le 0 \\ d_{a_U} &= 1/2 - 1/2 d_a \\ d_{a_L} &= 0 \end{aligned}\right\}$$

$$\left.\begin{aligned} i_{a_{ref}} &\ge 0 \\ d_{a_U} &= 0 \\ d_{a_L} &= 1/2 + 1/2 d_a \end{aligned}\right\}$$

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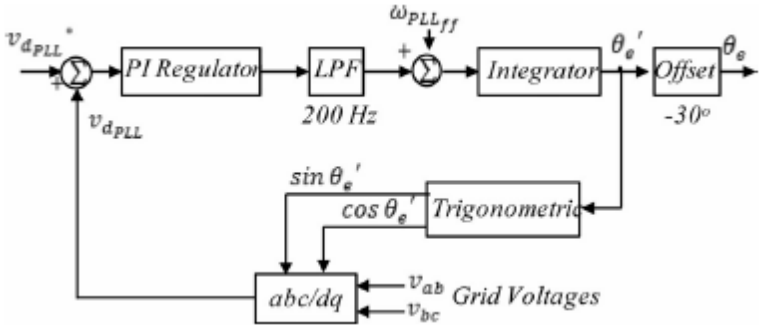
reference duty cycle, and $d_{a\,U}$, $d_{a\,L}$ are the phase *a* upper and lower switch duty cycles, respectively, with no dead time re-quired. The dual boost circuit integrates two active switches per phase or six active switches for a three-phase system without having two switches in series for each phase leg; in consequence, the shoot-through failure is avoided. This distinguished feature makes the dual boost topologies attractive due to their high re-liability. Generally, a hard-switched conventional three-phase circuit utilizes the insulated gate bipolar transistors (IGBTs) rather than the metal–oxide—semiconductor field-effect tran-sistors (MOSFETs) as the main switch because of poor reverse recovery characteristics of their body diodes. However, in dual boost circuit, the MOSFETs can be employed with three-phase circuits as their body diodes do not conduct current. The use of MOSFETs allows higher switching frequencies where the size of the passive components can be significantly reduced. Furthermore, the turn-off and conduction losses can be substan-tially reduced with proper switch selection.



Circuit diagram of the digital PLL.

Fig. 2 illustrates the proposed control strategy of the three-phase dual boost rectifier. This digital control system is based on the *dq0* synchronous rotating reference frame that is referenced to the grid phase-to-neutral voltage $v_{a\,n}$ through a phase-locked loop (PLL). The PLL circuit is designed in the *dq0* synchronous frame as shown in Fig. 3 along with its designed parameters. The voltage reference of the PLL control loop $v_{d^*\mathrm{PLL}}$ is set to zero and an angle offset (30°) has been added to compensate for the phase difference between line-to-line and phase-to-neutral grid voltages. The control system incorporates two decoupled inner current loops (*d*-axis and *q*-axis) to control the ac input current and a superimposed outer voltage loop to control the dc- link voltage. The outer voltage loop generates the *q*-axis current reference, whereas the *d*-axis current reference is set to zero to get unity power factor at the ac side. In some cases, the *d*-axis current reference is set to a negative value to compensate for the reactive power component of the input current; this reactive power can be created due to the insertion of the electromag-netic interference (EMI) filter

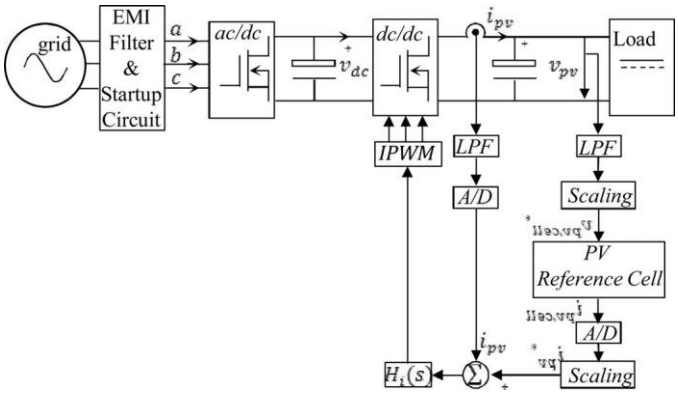


FIG Control strategy block diagram for the three-phase dc–dc converter.

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at certain conditions, and thus allowing larger ripple current for individual phase currents or smaller size inductors [57]. This allows the control system to be designed with fast transient response time which is necessary for PV source simulators. Furthermore, the fundamental frequency of the output ripple current is n times the switching frequency allowing a small output capacitor to be used. Fig. 5 shows the proposed control strategy of the three-phase dc–dc interleaved buck converter. This hybrid control system incorporates two control loops, an outer analog loop and an inner digital loop. The purpose of the outer analog loop is to generate a precise real-time reference current whereas the inner digital loop aims to control the total average inductor current i_L of the converter to match the actual current–voltage characteristics of the reference cell and achieve fast dynamic response to load disturbances. The real-time ana-log reference generation is conceived by the circuit in Fig. 6. This analog circuit controls the output voltage of an illuminated PV cell $v_{pv,cell}$ in order to generate the reference current $i_{pv,cell}$. This analog implementation of the reference generation circuit is accurate, simple, and flexible. Modeling, control, and design

III. CONTROL SYSTEM AND POWER STAGE DESIGN METHODOLOGY

A. Modeling, Control, and Design of the AC–DC Rectifier Stage

The dual control system of the ac–dc rectifier stage aims to control the dc-link output voltage, control and shape the ac input current, achieve unity power factor at the input, and attain a fast dynamic response to load disturbances. This system is imple-mented with Texas Instruments DSP (Model: TMS320F28335), which is a 32-bit high-performance floating point controller. The design of the rectifier control loops in frequency domain (q-axis and d-axis control loops) requires the derivation of four models in state-space representation format: 1) the switching model as in (5) and (6); 2) the large-signal model in the *abc* frame as in and (8); 3) the large-signal model in the *dq0* frame as in (9); and 4) the small-signal model as in (10). Park's transformation matrix is used to transform the *abc* frame to the *dq0* frame. The *dq0* frame reduces the three ac quantities into a two dc quanti-ties, and hence simplifies mathematical operations. Based on the derived models (switching, large, and small signal), the decou-pled control to q-axis input-current transfer function G_{id} (s) in *dq0* synchronous rotating reference frame assuming continuous conduction mode (CMM) operation is derived as in (11) The derived switching model is based on the switching com-binations of the three-phase switching functions s_a , s_b , and s_c . If phase a upper switch is on, s_a is 1, and if phase a lower switch is on, s_a is 0. i_a , i_b , and i_c are input phase currents, v_{an} , v_{bn} , and v_{cn} are grid input phase voltages, d_a , d_b , and d_c are phase duty cycles, i_{ds} and i_{qs} are the d-axis and q-axis com-ponents of the input phase currents, v_{dg} and v_{qg} are the d-axis and q-axis components of the grid input phase voltages, v_{dc} is the dc-link voltage, d_d , d_q are the d-axis and q-axis components of the phase duty cycles, T_i (s) is the angular frequency, c_{dc} is the dc-link capacitance, L_{in} is the phase boost inductance, R is the equivalent resistance of the dc–dc converter stage, and P_o is the rectifier steady-state output power.

The design procedure of the q-axis and d-axis current loop controllers is identical. A conventional linear proportional– integral (PI) controller G_i (s) is suitable to realize input current fast dynamics and minimize steady-state error. The controller is designed around the peak MPP of the dc–dc converter stage to maintain full control bandwidth.

Fig. 7 shows the frequency response of the compensated cur-rent loop gain T_i (s) including digital time delay. The digital time delay is modeled as e^{-sT_s} (T_s is the sampling time). The de-signed controller attains a 2.5 kHz cross-over frequency, which is about one-tenth below the switching frequency (33 kHz) and 88° phase margin through placing the compensator zero at a frequency below the resonant frequency of the system plant

may cause zero crossing distortion because the system holds high phase margin at frequencies lower than the designed band-width. After closing the current loops (q-axis and d-axis), the outer voltage loop that controls the dc-link voltage can be closed. The dc-link voltage to the q-axis reference current transfer func-tion can be derived as follows:

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$$G_{vi}(s) = \frac{T_{icl}(s)}{C_{dc}s + P_o/V_{dc}^2}$$

$$T_{icl}(s) = \frac{T_i(s)}{1+T_i(s)} = \frac{G_i(s)G_{id}(s)}{1+G_i(s)G_{id}(s)}$$

where $T_{ic\,l}$ (s) is the closed-loop q-axis current controller transfer function. A PI controller G_v (s) is used as a voltage compen-sator to regulate the dc-link voltage. Fig. 7 shows the frequency response of the compensated outer voltage loop gain G_v (s) including digital time delay, as well. In three-phase rectifier systems, the voltage loop is usually designed at a frequency one decade below 360 Hz so that the controller does not respond to the sixth harmonic of line frequency at the dc-link [58]. There-fore, the voltage loop is designed to achieve a 50 Hz cross-over frequency and 93° phase margin. Table I shows the designed current and voltage compensator parameters of the inner cur-rent loops and outer voltage loop of the rectifier stage.

The rectifier stage input inductance L_{in} is designed in CCM to allow 10% peak-to-peak input current ripple. Three stackable toroid powder cores with 60 μ permeability (Model: Kool Mμ 77192 A) has been selected to obtain the required inductance value. The inductor was built and experimentally tested using a two-pulse test circuit to verify its inductance value along with its saturation current characteristics. Fig. 8 shows the inductor current and voltage waveforms.

B. Modeling, Control, and Design of the DC–DC Converter Stage

The control system of the dc–dc converter stage aims to con-trol the total output inductor current $i_{p\,v}$ of the converter through an inner digital loop. To design the dc–dc converter control sys-tem, the large and small signal models of the converter are derived assuming a resistive-type load as in (14) and (15) and as a voltage-type load as in (16) and (17), respectively. Based on the derived models, the control to the total-current trans-fer function H_{id} (s) including circuit parasitics is given as in

where $i_{p\,v}$ is the total inductor current, v_C is the output capacitor voltage, d is the converter main duty cycle, L_o is the output phase inductance ($L_o = L_1/3 = L_2/3 = L_3/3$), C_o is the output ca-pacitance of the converter stage, r_l and r_c are the equivalent se-ries resistance of the phase inductance and output capacitance, respectively. R is the equivalent load resistance of the power conditioning system. A proportional—integral–derivative (PID) controller H_i (s) is selected to achieve fast dynamic response of the current loop assuming either a resistive-type load or a voltage-type load. Although, the cutoff frequency of the output filter is a key limitation factor against high system control loop bandwidth, the use of the three-phase interleaved buck converter allows the use of small phase inductors and output capacitor that improves system transient response. The designed compensator achieves a 4.2 kHz cross-over frequency, which is about one-eighth below the switching frequency (33 kHz) and 104° phase margin. Fig. 9 shows the frequency response of the uncompen-sated system plant H_{id} (s) and the compensated current loop gain L_i (s) including digital time delay for a resistive-type load and for a voltage-type load. The current loop gain L_i (s) has been measured and verified using a Venable frequency response analyzer (Model: 3120). The control system includes an outer

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TABLE I
DESIGNED CONTROLLERS PARAMETERS OF RECTIFIER AND CONVERTER STAGES

ac-dc Rectifier Stage (Boost)		
Control Loop	Controller Format	Design Parameters
Inner Current Loop $G_i(s)$	$k\frac{(s/\omega_z+1)}{s}$	$k = 20.64$ $\omega_z = 526\ rad/s$
Outer Voltage Loop $G_v(s)$	$k\frac{(s/\omega_z+1)}{s}$	$k = 7$ $\omega_z = 9\ rad/s$
dc-dc Converter Stage (Buck)		
Inner Current Loop $H_i(s)$	$k\frac{(s/\omega_z+1)(s/\omega_z+1)}{s}$	$k = 39.2$ $\omega_z = 11.05\ krad/s$
Outer Reference Loop $H_v(s)$	$k\frac{(s/\omega_z+1)}{s(s/\omega_p+1)}$	$k = 42.19$ $\omega_z = 71.4\ krad/s$ $\omega_p = 86.8\ krad/s$

analog reference loop that generates the reference value to the digital inner current loop. The outer loop includes the reference-cell circuitry that is designed to match the response of the actual solar cell. An analog controller H_v (s) is implemented to obtain 200 Hz cross-over frequency and 90° phase margin. To limit the speed of the outer loop, a low-pass filter (LPF) is added in series with the reference-cell circuitry to control the converter overall bandwidth. This control loop bandwidth will be changed to optimize the converter overall bandwidth as will be discussed in the experimental results section. Fig. 10 shows the measured loop gain of the reference generation circuit. Table I summa-rizes the parameters of the designed controllers of the converter stage.

$$L_{\text{phase}} = \frac{V_{dc}V_{\text{PV}} - V_{\text{PV}}^2}{nV_{dc}f_s\Delta I_{\text{PV}}}$$

V. CONCLUSION

A new type of PV source simulator has been proposed and thoroughly described. The proposed simulator has been used to precisely emulate the static and the dynamic characteristics of actual PV systems at different load and environmental con-ditions including the effect of partial shading. The simulator uses a real-time analog reference circuit to extract the reference curves which are then digitally processed to emulate the char-acteristics of a high power system. The proposed simulator has been successfully used to evaluate the dynamic performance of a commercial solar power inverter and its MPPT algorithm in steady-state and transient conditions. The measured closed-loop output impedance has been verified at different operating regions including, constant current and constant voltage. The impedance profile of the proposed simulator matches the impedance of ac-tual PV generator.

The proposed PV source simulator consists of two power switching stages. The three-phase ac–dc rectifier stage is a new dual boost topology that is reliable and highly efficient, whereas the second-stage, the three-phase dc–dc converter helps improve system transient response though producing low output voltage and current ripples. The experimental results illustrate the pro-posed system has achieved high two-stage efficiency and fast transient response time relative to MPPT algorithms.

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